CLAIMS

WE CLAIM:

1. An integrated circuit fabricated on a single substrate comprising:

a data bus; and

purpose-specific functional units operatively connected to said data bus, said functional units comprising:

a JPEG decoder;

a compressed bi-level expander;

a halftoner; and

a printhead interface.

2. An integrated circuit according to claim 1, further comprising a general-purpose processor operatively connected to said data bus for controlling said functional units, wherein said processor is operative to run software that coordinates said functional units to receive, expand and print pages.

3. An integrated circuit according to claim 2, wherein said processor is operative to print pages in streaming mode.

4. An integrated circuit according to claim 2, wherein said processor is operative to print pages in single-page mode when the size of said received pages exceeds a memory threshold.

5. An integrated circuit according to claim 4, wherein said memory threshold is 3MB.

6. An integrated circuit according to claim 1, wherein said JPEG decoder and said compressed bi-level expander are operative to decompress in parallel both a bi-level layer and a contone layer.

7. An integrated circuit according to claim 1, wherein said halftoner is operative to halftone contone color data to a bi-level color layer, and then to composit a bi-level black layer over said bi-level color layer.

8. An integrated circuit according to claim 1, wherein said halftoner is operative to halftone contone CMYK data to a bi-level CMYK layer, and then to composit a bi-level black layer over said bi-level CMYK layer.

9. An integrated circuit according to claim 2, wherein said processor is operative to transfer bi-level CMYK data to said printhead interface at a constant required rate.

10. An integrated circuit according to claim 2, wherein said processor is operative to expand pages in real time during printing.

11. An integrated circuit according to claim 2, further comprising a multi-channel DMA controller operatively connected to said data bus, wherein each of said functional units further comprises one or more on-chip input and/or output FIFOs, and wherein each FIFO is allocated a separate channel in said multi-channel DMA controller.

12. An integrated circuit according to claim 11, wherein said DMA controller is operative to interrupt said processor when a data transfer is complete.

13. An integrated circuit according to claim 12, wherein said compressed bi-level expander unit comprises:

a bitstream decoder;

a state machine operatively connected to said bitstream decoder;

edge calculation logic operatively connected to said state machine;

two runlength decoders operatively connected to said edge calculation logic; and

a runlength (re)encoder operatively connected to said edge calculation logic.

14. An integrated circuit according to claim 13, wherein said state machine is operative to control said edge calculation logic in response to codes supplied by said bitstream decoder.

15. An integrated circuit according to claim 1, wherein said compressed bi-level expander is an EDRL expander.